REMARKS/ARGUMENTS

In the Office action dated May 31, 2005, the Examiner rejected claims 1-16, al of the claims in the Application, under 35 U.S.C. § 112, 2d paragraph, for a variety of reasons.

Claims 1-16 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of copending Application Serial No. 10/676,983 (2005/0070114-A1, for Selective Etching Processes for In₂O₃ Thin Films in FeRAM Device Applications, of Li et al.) and copending Application Serial No. 10/780,919. Applicants hereby indicate their willingness to provide a terminal disclaimer as required upon allowance of claim(s) in this applications.

The Examiner rejected claims 1-6 and 9-14 under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,825,519 B2 of Li et al. in combination with U. S. Patent No. 5,003,428 of Shepard. Claims 7, 8, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over '519 in combination with '428 and in combination with U. S. Patent No. 6,664,116 B2 of Li et al.

In the Specification, pages 1 and 5 have been amended to correct typographical errors.

In the Claims, claims 1, 9 and 11 have been amended to overcome the 35 U.S.C. § 112, 2d paragraph rejections.

New claims 17-20 have been added.

The Invention

The invention is a method of forming an indium-containing thin film on a silicon substrate, patterning the indium-containing thin film and depositing a layer of ferroelectric

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material on the indium-containing thin film in a process which eliminates the need for subsequent patterning of the ferroelectric layer. The use of the indium-containing thin film as a bottom electrode for a ferroelectric stack allows for much faster deposition of the ferroelectric material on the indium-containing thin film than on the surrounding material, thus simultaneously depositing and patterning the ferroelectric. See page 7, table 3 of the Specification.

The Applied Art

The Examiner has applied two patents by Li et al., which include all of the inventors hereof. U. S. Patent No. 6,825,519 B2 describes selective deposition of a PGO thin film, but, as the Examiner correctly points out, does not teach use of an indium-containing bottom electrode. '519 and U. S. Patent No. 6,664,116 B2 describes use of a ferrorelectric seed layer.

U. S. Patent No. 5,003,428 of Shepard describes various electrode materials which may be used in ceramic oxide capacitors. Contrary to the Examiner's contention, '428 does not teach use of indium oxide and indium tin oxide as a functional thin film ceramic capacitor. The entire of the text of the applied portion of '428 states:

Indium oxide and indium-tin oxide have also been used as electrode materials for thin film ferroelectric ceramic oxide capacitors. However, these compounds have insufficient conductivity to perform well as electrodes for such capacitors in integrated circuits, where it has always proved desirable to have conductive materials be as conductive as possible so that extended lengths can be used without causing significant voltage drops in the circuit. Emphasis added.

The Claims

Claim 1 has been amended to eliminate the final element to overcome a 35 U.S.C. § 112, 2d paragraph rejection. With respect to the other 35 U.S.C. § 112, 2d paragraph rejection

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regarding Applicants' use of the word "thin," "thin" is defined in the Specification, page 3, lines 11-13, as being a layer having a thickness of between about 10 nm and 2 µm. Clearly, one of ordinary skill in the art can determine from the Specification, the meaning of "thin," and the 35 U.S.C. § 112, 2d paragraph rejection should be withdrawn.

Turning to the merits regarding claim 1, the Examiner contends that a combination of '519 and '428 render the claim unpatentable, because the Examiner's combination is a ferroelectric device having an indium-containing bottom electrode. This is clearly not taught by the Examiner's combination. As set forth above, the applied portion of '428 states that indium-containing materials have been used as electrodes, but don't work, teaching away from Applicants' invention. Applicants, through the method of their invention, have fabricated a ferroelectric device having an indium-containing bottom electrode where others have failed. Claim 1 is allowable over the applied art.

The Examiner rejected claims 2 and 3 under 35 U.S.C. § 112, 2d paragraph, stating that the language was "confusing." Applicants are somewhat perplexed by this rejection: claim 1 recites a step of preparing a silicon substrate; claim 2 recites forming an oxide layer on the silicon substrate as part of that step; claim 3 recites preparing a high-k oxide on the silicon substrate as part of the preparing step. The Specification, page 3, lines 8-11, states that, as part of preparing a silicon substrate, an oxide layer or a high-k oxide layer may be formed on the silicon substrate. The subsequent step of claim 1 states that an indium-containing thin film is deposited. Thus, the indium-containing thin film may be deposited on silicon, on an oxide layer formed on silicon, or on a high-k oxide formed on silicon. The Examiner also rejected claim 3 under 35 U.S.C. § 112, 2d paragraph, stating that "high-k" was indefinite. Several examples of

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high-k materials are provided in the Specification, page 3, lines 10-11, which provide sufficient definiteness to one of ordinary skill in the art. The 35 U.S.C. § 112, 2d paragraph rejections of claim 2 and 3 should be withdrawn. Claims 2 and 3 are allowable with their allowable parent claim.

Claim 4 recites that the patterning step includes etching the indium-containing thin film. There is no specific language in the applied references regarding this rejection, however, as the Examiner combined references do not teach formation of a functional indium-oxide containing electrode, the combined references cannot teach or suggest etching such an electrode. Claim 4 is allowable over the applied art, or is alternately allowable with its allowable parent claim.

Claim 5 stands rejected under 35 U.S.C. § 103(a), although no specific portion of the references were applied to this rejection. The only reference containing anything regarding a "trench" is '519, which describes a standard STI process, which does not render the method of the invention obvious. Claim 5 is allowable over the applied art.

Claims 6-8 are allowable with their allowable parent claims.

Claim 9 has been amende to overcome the 35 U.S.C. § 112, 2d paragraph rejections by inclusion of quantitative parameters to define "thin" and to eliminate the final "completing" step. As noted in connection with claim 1, the Examiner combined references do not teach a functional indium-containing thin film electrode, and does not specifically teach use of In_2O_3 as a thin film. Claim 9 is allowable over the applied art.

Claim 10 is allowable for the reasons set forth in connection with claim 2.

Claim 11 has been amended to recites specific high-k materials, and the claim thus overcomes the 35 U.S.C. § 112, 2d paragraph rejection, and is allowable for the reasons set forth

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in connection with claim 3.

Claims 12-16 are allowable for the reasons set forth in connection with claims 4-8, respectively.

New claim 17 includes the limitations of allowable claims 9 and 10, and includes additional limitations describing the patterning and etching of the In₂O₃ layer to provide a form for the subsequently deposited PGO layer. The claim is believed to be allowable over the applied art.

New claims 18-20 are allowable for the reasons set forth in connection with claims 6-8.

In light of the foregoing amendment and remarks, the Examiner is respectfully requested to reconsider the rejections and objections stated in the Office action, and pass the application to allowance. If the Examiner has any questions regarding the amendment or remarks, the Examiner is invited to contact the undersigned.

Provisional Request for Extension of time in Which to Respond

Should this response be deemed to be untimely, Applicants hereby request an extension of time under 37 C.F.R. § 1.136. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any over-payment to Account No. 19-1457.

Respectfully submitted,

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